THAT WHICH IS CLAIMED IS:

1. Configurable electronic circuit, characterized in that it includes at least one tile (TL) including at least two individual cells (CEL1, CEL10) interconnected, each individual cell (CEL1) having a multiplier (MX1), an arithmetic and logic unit (ALU1) capable of performing at least one arithmetic and/or logic function that can be selected from a predetermined set of arithmetic and/or logic functions, a vertical bus (BSV1), a first configurable switching block (CBX1A, CBX1B) connected to the vertical bus and to the inputs of the multiplier, a second configurable switching means (CBX2) connected to the vertical bus and to the output of the multiplier, a third configurable switching means (CBX3) connected to the vertical bus and to the output of the multiplier (MX10) of the other individual cell (CEL10), a second configurable switching block (CBX4A, CBX4B) connected to the vertical bus and to the inputs of the arithmetic and logic unit, a fourth switching means (CBX5) connected to the vertical bus and to the output of the arithmetic and logic unit, a carry propagation bus (BPR) linking the two arithmetic and logic units, a terminal switching block (SBX1) connected to the vertical bus, and a horizontal bus (BH) linking the two terminal switching blocks.

2. Circuit according to Claim 1, characterized in that each multiplier (MX1) is an m*n bit multiplier having two inputs intended to receive two words of m and n bits respectively, and an output intended to deliver an output word of m+n bits, in that

the second switching means (CBX2) of a first individual cell (CEL1) of the tile is intended to receive n bits of the output word delivered by the multiplier (MX1) of the first cell, in that the third switching means (CBX3) of this first individual cell (CEL1) is intended to receive n bits of the output word delivered by the multiplier (MX10) of the second individual cell (CEL10) of the tile, in that the second switching means (CBX20) of the second individual cell (CEL10) is intended to receive m bits of the output word delivered by the multiplier (MX10) of this second cell, and in that the third switching means (CBX30) of this second individual cell (CEL10) is intended to receive m bits of the output word delivered by the multiplier (MX1) of the first individual cell (CEL1).

3. Circuit according to Claim 2, characterized in that each bus (BSV1, BSV10, BH) of the tile is capable of conveying words having a number of bits at least equal to the lowest common multiple of m and of n.

4. Circuit according to Claim 2 or 3, characterized in that m is equal to n, and in that each bus (BSV1, BSV10, BH) of the tile has p tracks of n bits, p being an integer greater than 1.

5. Circuit according to one of the preceding claims, characterized in that it includes several tiles (TL1-TL4) interconnected.

6. Circuit according to Claim 5, characterized in that the tiles (TL1-TL4) are connected in quincunx form.

7. Circuit according to Claim 5 or 6, characterized in that it additionally includes a sign extension module (MES12, MES14) connected to two adjacent tiles of the same horizontal row, this sign extension module being connected between the arithmetic and logic unit of an individual cell of a first tile and the vertical bus of the individual cell of the second tile, immediately adjacent to the said individual cell of the first tile.

8. Circuit according to one of the preceding claims, characterized in that the tile furthermore includes an additional row (RS) having two vertical bus extensions (PBSV1, PBSV10) connected to the two terminal switching blocks respectively, two additional configurable terminal switching blocks (SBX1S, SBX10S) connected to the two vertical bus extensions respectively, an additional horizontal bus (BHS) connected between the two additional terminal blocks, two additional arithmetic and logic units (ALU1S, ALU10S) connected to the two vertical bus extensions, respectively, via additional switching means, and one additional carry propagation bus (BPRS) connected between the two additional arithmetic and logic units.

9. Circuit according to Claim 8 taken in combination with one of Claims 5 to 7, characterized in that it has specific buses (BSPL1, BSPL10) interlinking

the additional arithmetic and logic units of adjacent tiles of the same column.

10. Circuit according to one of the preceding claims, characterized in that it is produced in the form of an integrated circuit.